Lab 5

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Prelab:

A picture containing athletic game, sport

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Purpose:

The purpose of lab 5 was to design a circuit with multi-level NAND gates and a circuit with multi-level NOR gates that were equivalent to a given combinational circuit.

Lab Procedure:

We started the lab by opening Vivado and creating an RTL project that was set to ‘VHDL’ target language. We continued by creating a design source file called Lab5 with I/O ports for the file. The inputs were a, b, c, d, and e and the outputs were f1, f2, and f3. We then wrote 9 lines of code that would simulate the boolean expressions for f1, f2, and f3 from the prelab.

Next, we created a simulation file titled multiLevel, copy and pasted the I/O from Lab5 into multiLevel, created std\_logic signals for the inputs and outputs, and also added a port map to Lab5. Finally, we added our 32 test cases into the program(00000 – 11111).

We then ran the Behavioral Simulation and took note of the waveform output, created one final program called multiLevelTest that would allow us to enter our inputs on a Basys 3 board, then ran Synthesis, Implementation, and finally Generated Bitstream. We then connected the Basys 3 board to the computer and manually tested the outputs on it.

Vivado Code-

Graphical user interface, text, application, email

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Description automatically generatedGraphical user interface, text, application

Description automatically generated

Basys 3 Board-

Input: 01111

A picture containing text, electronics, circuit

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Input: 00110

A picture containing electronics

Description automatically generated

Input: 01100

A close-up of a computer chip

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Input: 11111

A picture containing text, electronics, circuit

Description automatically generated

Bitstream-

A screenshot of a computer

Description automatically generated with medium confidence

Conclusion:

In this lab, we made 2 circuits, one with multi-level NAND gates and one with multi-level NOR gates. The results of this lab supported the prelab showing that the combinational circuit, the equivalent circuit with NAND gates, and the equivalent circuit with NOR gates all had the same output for every input. We were able to manually test these with the Basys 3 board which had switches we could move between high and low input.

Finally, I believe physically constructing a circuit is more beneficial to my learning.

Observations:

The main observation I have to improve my performance on future experiments would be to double check the written code in programs. During this lab, I messed up on one of the outputs and put C instead of B for an input.